

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims

1-11. (Cancelled)

12. (New) A method in a telecommunication or data communication network of reducing phase jumps in a frame synchronisation signal when switching from a first reference signal to a second reference signal, said method comprising the steps of:

generating a first and a second master reference signal phase locked to the first and the second reference signals, respectively, each master reference signal having a frequency n times the frequency of the corresponding reference signal;

selecting one of the master reference signals by a selection signal;

dividing the frequency of the selected master reference signal back to the frequency of its corresponding reference signal; and,

inputting the frequency divided signal into a Phase-Locked Loop circuit for generating said frame synchronization signal.

13. (New) The method recited in claim 12, wherein in the selection step, the first master reference signal is selected when the selection signal is a low, and the second master signal is selected when the selection signal is high.

14. (New) The method recited in claim 12, wherein the dividing step is carried out by counting the number of periods of the selected master reference signal and outputting a pulse like in the corresponding reference signal for each n^{th} period of the selected master reference signal.

15. (New) The method recited in claim 12, wherein the periods of the master reference signal are longer than the delta period of maximum tolerable frequency deviation of the corresponding reference signal.

16. (New) The method recited in claim 12, wherein the frame synchronization signal is a master frame synchronization signal in a PDH system.

17. (New) A system in a node of a telecommunication or data communication network of reducing phase jumps in a frame synchronization signal when switching from a first reference signal to a second reference signal, said system comprising:

one or more circuits for generating first and second reference signals;

one or more circuits for generating a first and a second master reference signal phase locked to the first and the second reference signals, respectively, each with a frequency n times the frequency of the corresponding reference signal,

a multiplexer with the first and the second master reference signal as input in addition to a selection signal for selecting one of the master reference signals as the output of the multiplexer;

a divider dividing the frequency of the output of the multiplexer back to the frequency of the corresponding reference signal; and,

a Phase-Locked Loop circuit for generating the frame synchronization signal having the divider output signal as input.

18. (New) The system recited in claim 17, wherein the multiplexer selects the first master reference signal when the selection signal is low, and the second master reference signal when the selection signal is high.

19. (New) The system recited in claim 17, wherein the divider is a counter counting the number of periods of the output signal of the multiplexer outputting a pulse like in the corresponding reference signal for each n^{th} period of the output signal of the multiplexer.

20. (New) The system recited in claim 17, wherein the periods of the master reference signals are longer than the delta period of maximum tolerable frequency deviation of the corresponding reference signal.
21. (New) The system recited in claim 17, wherein the node is a switch.
22. (New) The system recited in claim 17, wherein the frame synchronization signal is a master frame synchronization signal in a PDH system.

* * *